DIGITAL LOGIC DESIGN PROJECT

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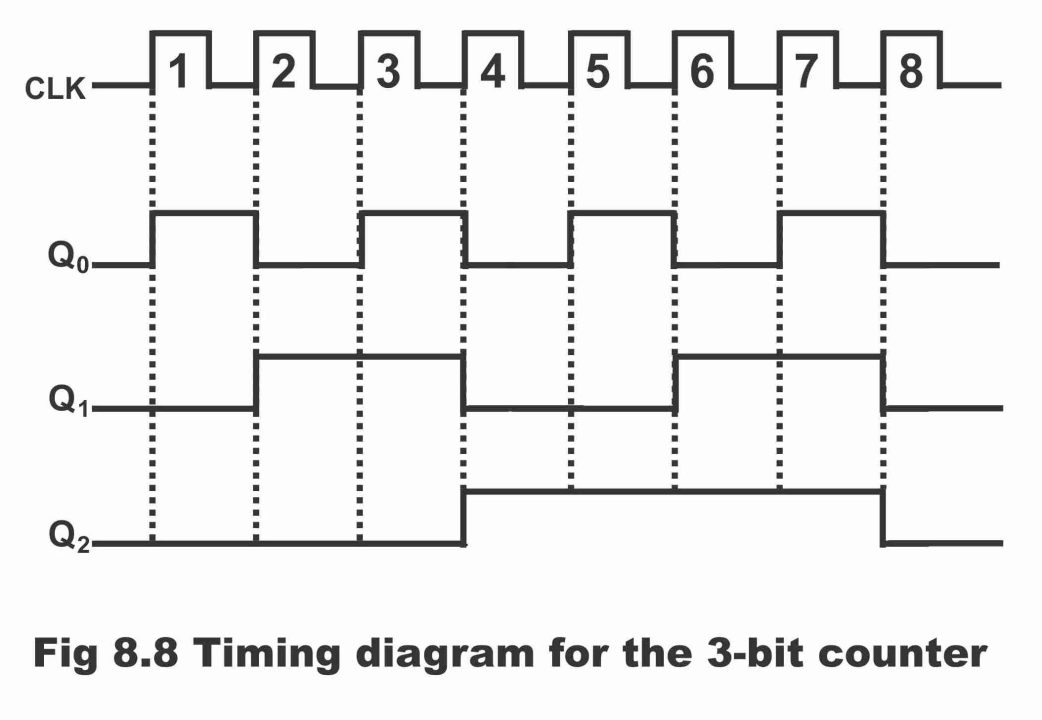
Project: Modulus 8 Counter

To start with our project, first we need to know what the function of our project is, our project's function is to count from 0-7 either in binary or decimal form. Now we need to know how many Flip Flops we will need to begin with our project knowing that 2n = 8 where n is the number of Flip Flops. In our case 3 flip flops. Concluding from that the maximum number 3 Flip Flops could count to is 7.

Then we start by drawing our State Transition Diagram:

Decimal Binary

Timing Diagram: (Postive Edge)



**1**

**0**

**1**

**1**

**1**

**1**

**1**

**1**

**1**

**1**

**1**

**1**

**1**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

**0**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Clock Pulse Table** | | | | |
| **No. Of Clock Pulse** | **Binary Counting System** | | | **Decimal Count** |
| **Clock Pulse** | **Qn2** | **Qn1** | **Qn0** | **Count** |
| **Initial** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **1** |
| **2** | **0** | **1** | **0** | **2** |
| **3** | **0** | **1** | **1** | **3** |
| **4** | **1** | **0** | **0** | **4** |
| **5** | **1** | **0** | **1** | **5** |
| **6** | **1** | **1** | **0** | **6** |
| **7** | **1** | **1** | **1** | **7** |
| **8** | **0** | **0** | **0** | **0** |

Table showing the relation between every clock pulse the output.

Now we will proceed by drawing the Truth Table for J-K Flip Flop:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Inputs flip flop and present state | | | outputs |  |
| J | k | Qn (Present State) | Qn+ (Next State) |
| 0  0 | 0  0 | 0  1 | 0  1 | No  Change |
| 0  0 | 1  1 | 0  1 | 0  0 | Reset  Mode |
| 1  1 | 0  0 | 0  1 | 1  1 | Set  Mode |
| 1  1 | 1  1 | 0  1 | 1  0 | Comp. of Present State |

We could extract our Flip Flop type Excitation Table from truth table in our case it is J-K:

|  |  |
| --- | --- |
| Qn  Qn+ | J K |
| 0 0 | 0 ϕ |
| 0 1 | 1 ϕ |
| 1 0 | ϕ 1 |
| 1 1 | ϕ 0 |

Now we could draw our State Table:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Qn2 | Qn1 | Qn0 | Qn+2 | Qn+1 | Qn+0 | J2 | K2 | J1 | K1 | J0 | K0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | ϕ | 0 | ϕ | 1 | ϕ |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | ϕ | 1 | ϕ | ϕ | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | ϕ | ϕ | 0 | 1 | ϕ |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | ϕ | ϕ | 1 | ϕ | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | ϕ | 0 | 0 | ϕ | 1 | ϕ |
| 1 | 0 | 1 | 1 | 1 | 0 | ϕ | 0 | 1 | ϕ | ϕ | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | ϕ | 0 | ϕ | 0 | 1 | ϕ |
| 1 | 1 | 1 | 0 | 0 | 0 | ϕ | 1 | ϕ | 1 | ϕ | 1 |

Now use our J-K inputs in the K-MAPS in the order of the K-Map:

Q1 Q0

Q2 00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0  0 | 1  0 | 3  1 | 2  0 |
| 4  ϕ | 5  ϕ | 7  ϕ | 6  ϕ |

0

1

J2=Q1Q0

Q1 Q0

Q2 00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0  ϕ | 1  ϕ | 3  ϕ | 2  ϕ |
| 4  0 | 5  0 | 7  1 | 6  0 |

0

1

K2=Q1Q0

Q1 Q0

Q2 00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0  0 | 1  1 | 3  ϕ | 2  ϕ |
| 4  0 | 5  1 | 7  ϕ | 6  ϕ |

0

1

J1=Q0

Q1 Q0

Q2 00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0  ϕ | 1  ϕ | 3  1 | 2  0 |
| 4  ϕ | 5  ϕ | 7  1 | 6  0 |

0

1

K1=Q0

Q1 Q0

Q2 00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0  1 | 1  ϕ | 3  ϕ | 2  1 |
| 4  1 | 5  ϕ | 7  ϕ | 6  1 |

0

1

J0=1

Q1 Q0

Q2 00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0  ϕ | 1  1 | 3  1 | 2  ϕ |
| 4  ϕ | 5  1 | 7  1 | 6  ϕ |

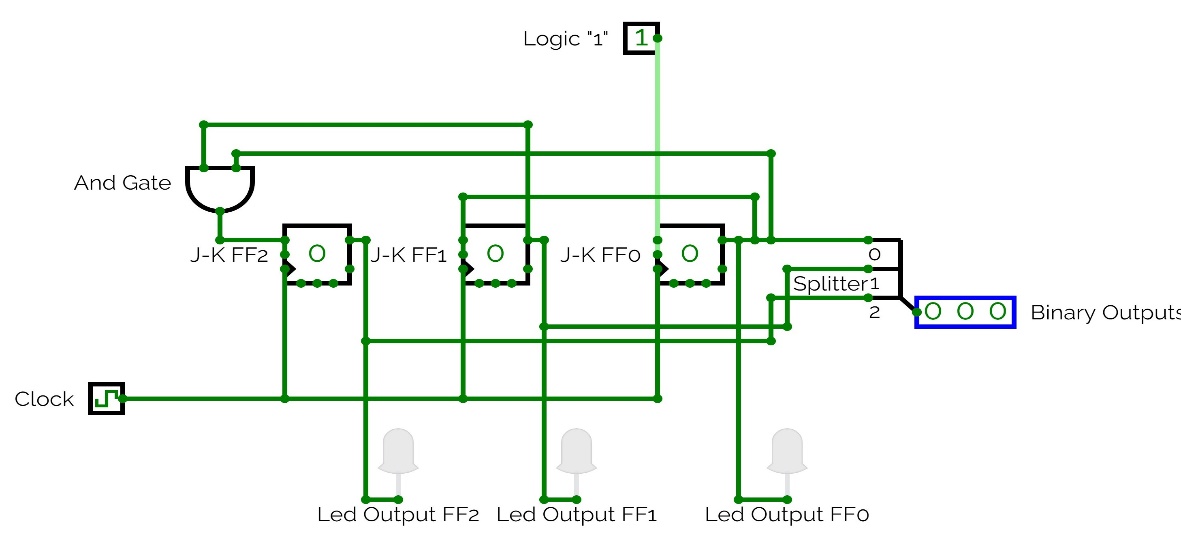
0

1

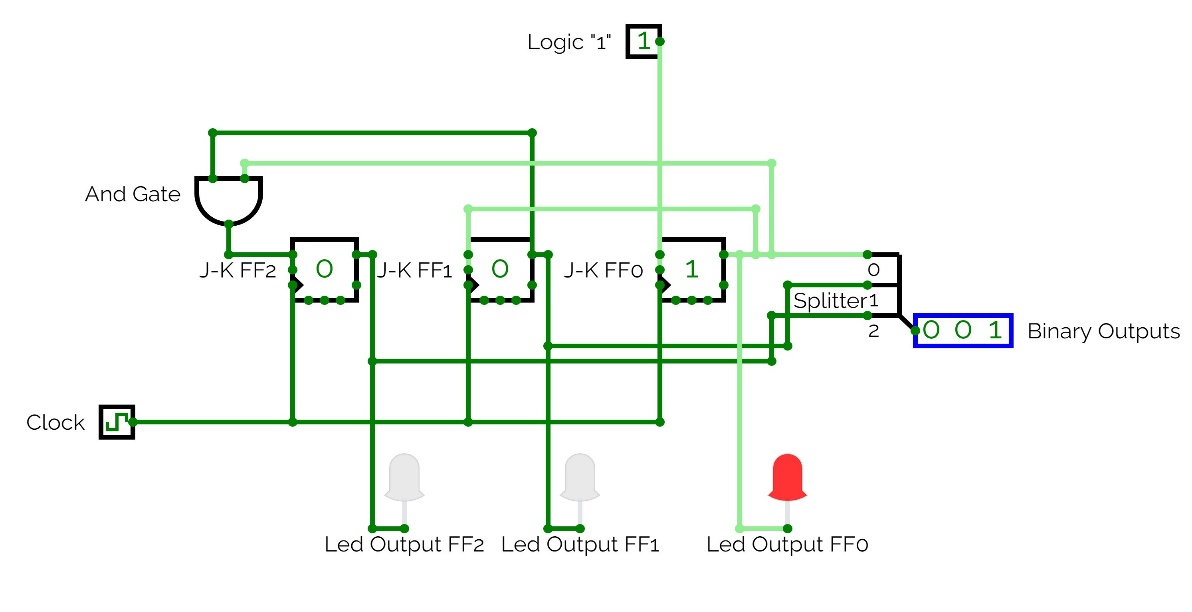
K0=1

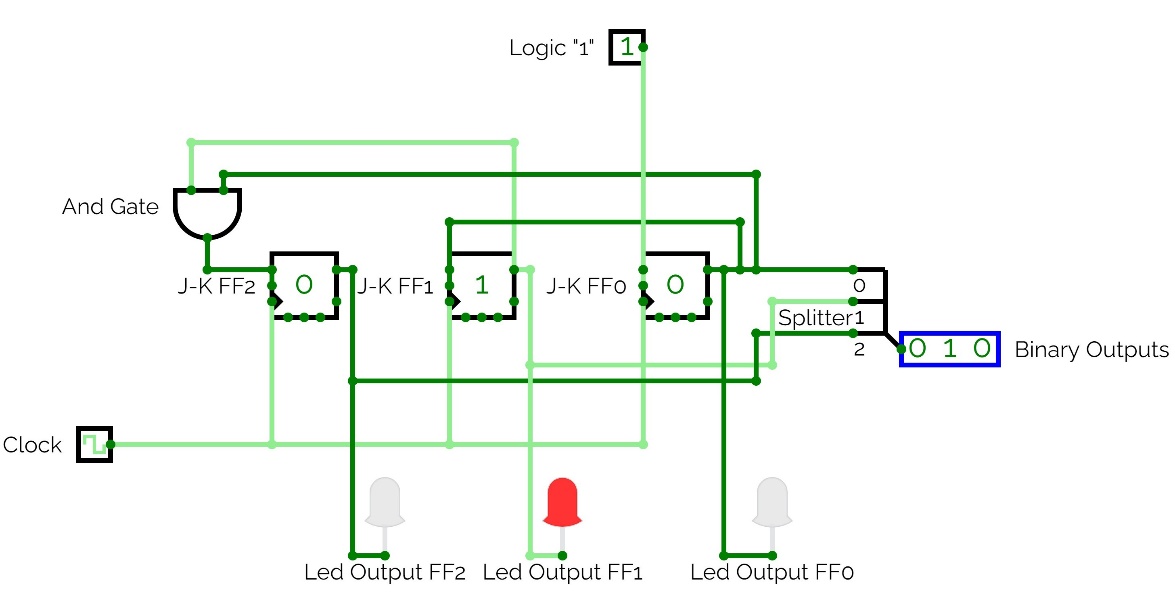
Implementation:

Here are the different outputs after Implementing our circuit.

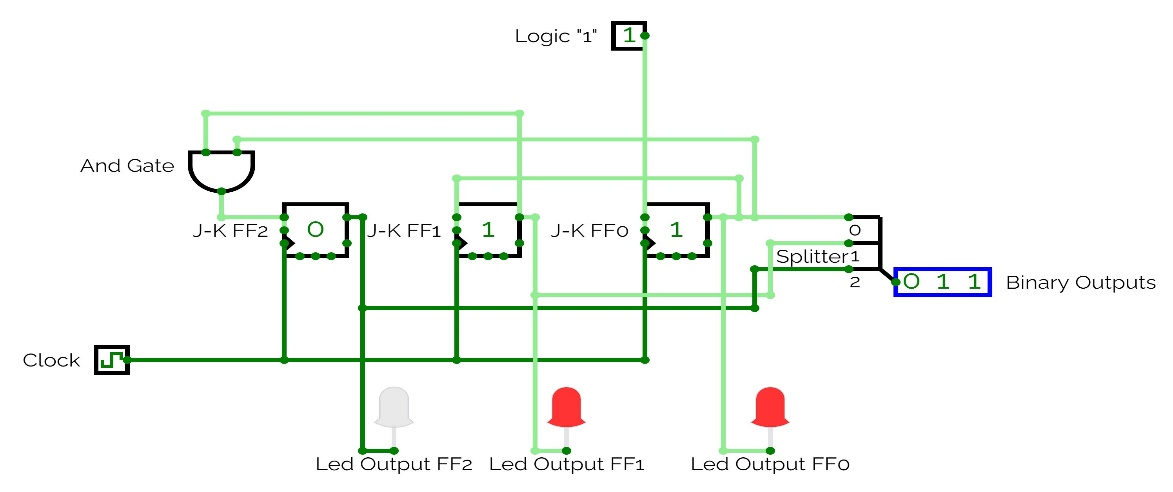


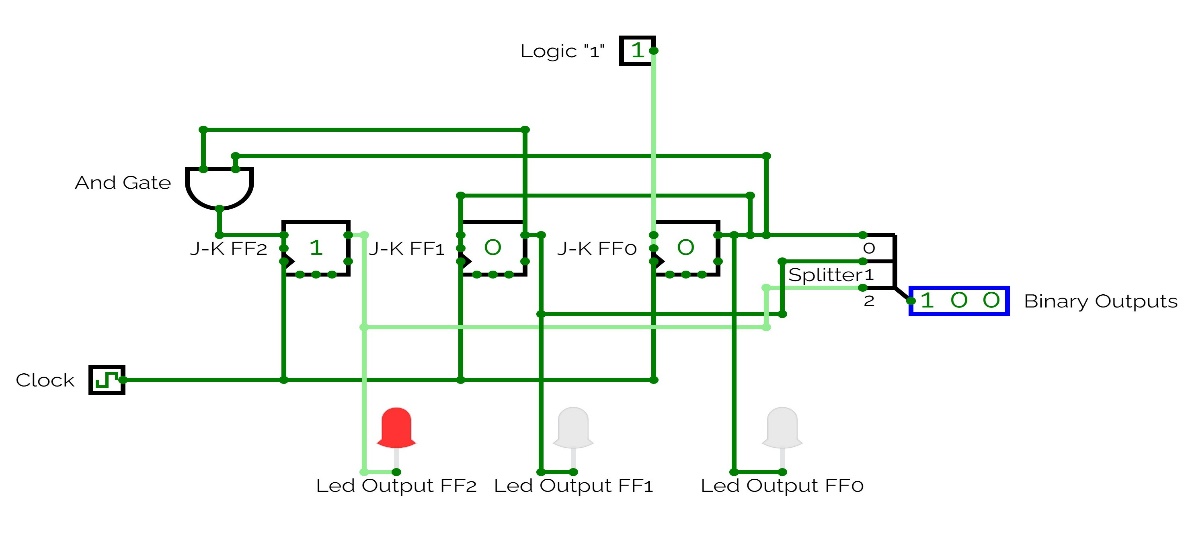
State: 0



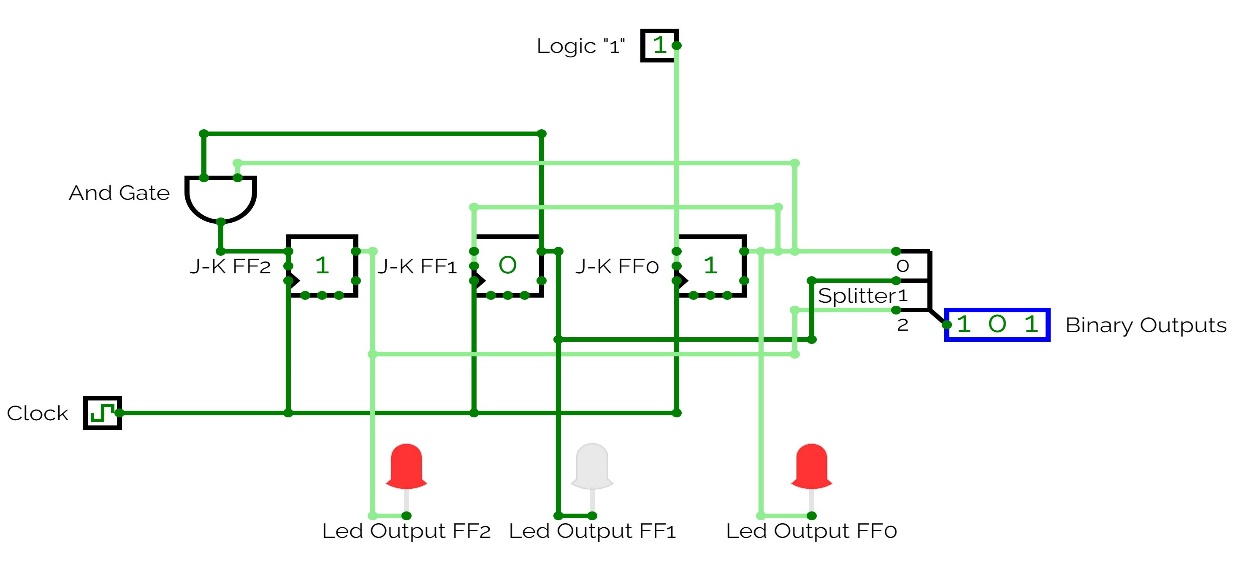
 State: 1

State: 2

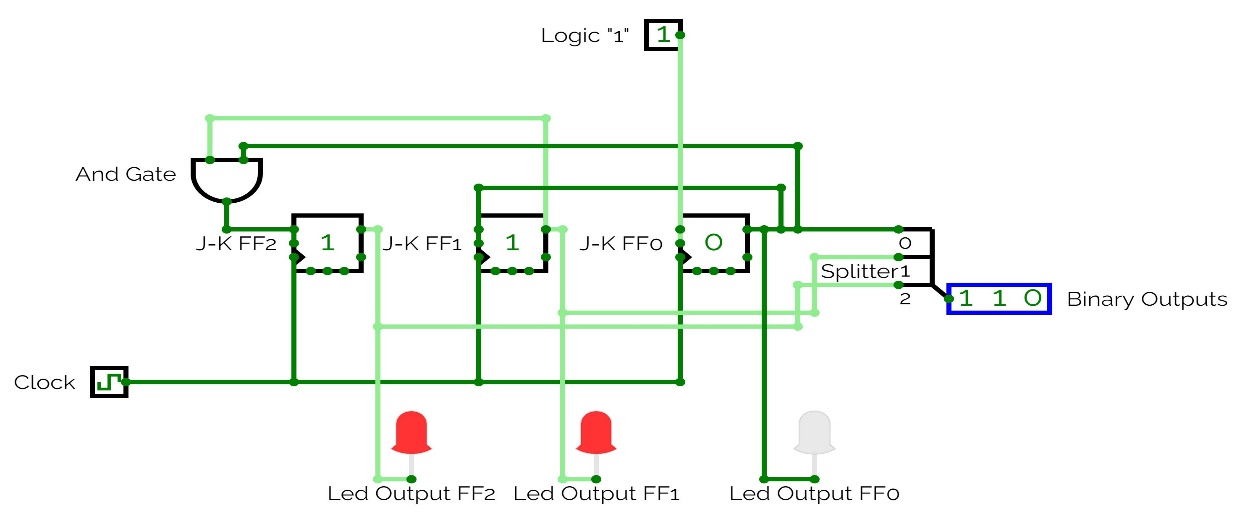
 State: 3



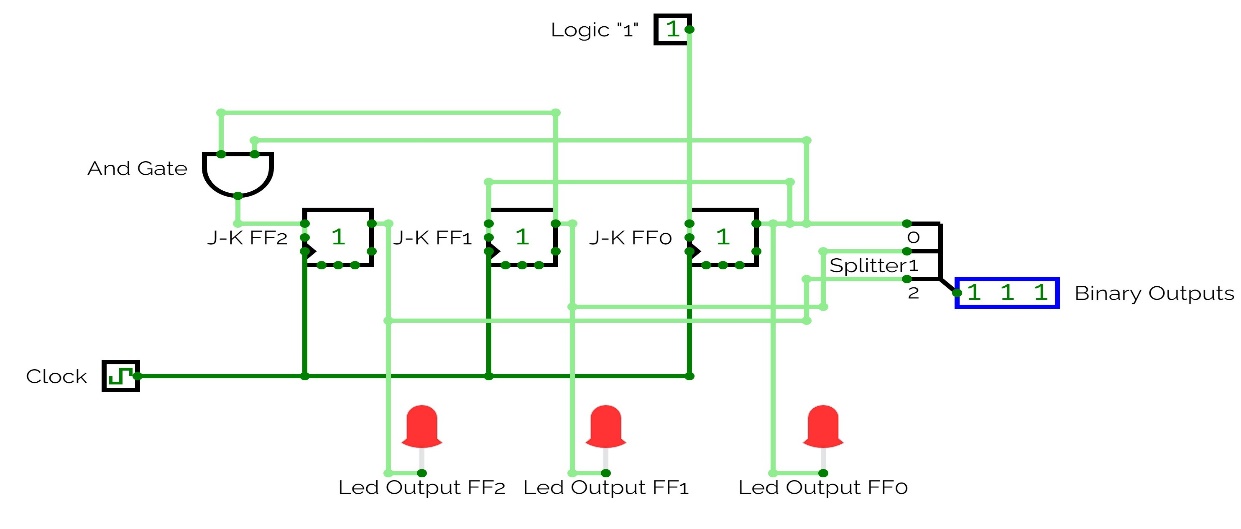
State: 4



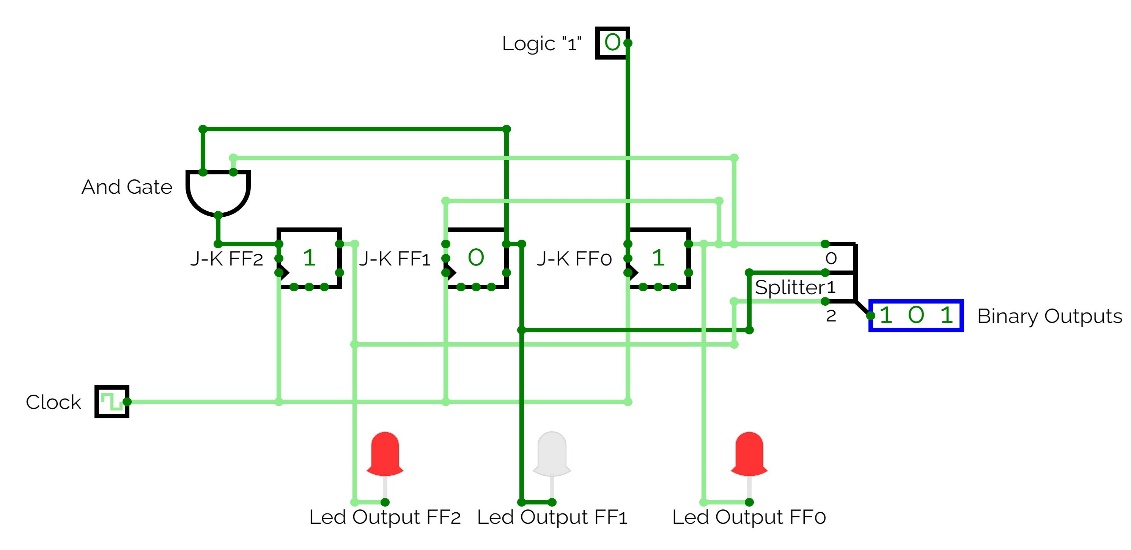
State: 5



State: 6



State: 7

If we apply Logic “0” on the first Flip Flop it will freeze at the last state when we first applied the Logic “0”.

